last cell of the machine and do not constitute any part of the output character sequence.

(c) In the interval defined by eqn. 3 the characters output from the last cell of the machine (when $p = m$) are the most significant characters of the product of the ith input mantissae.

A complete machine M must include carry states in the machine definition. Expanding the definition to include these states gives $\{S_p(n, X_0, X_1, X_2, Y_0, Y_1, Y_2, P, C) : p = 1, \ldots, m\}$. These carries are included in the computation as a carry–save operation.

Fig. 2 shows a cell which implements the recurrence relations used to define the machine M. A linear array of these

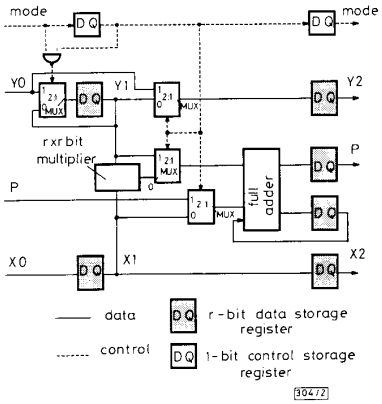

Fig. 2 *Character-serial floating point multiplier cell*

cells implements addition and multiplication of ordered 2-tuples. The maximum result mantissa denormalisation which can occur with normalised operands is one character. By placing a sign character in the exponent field, with guard characters on each side, sign-magnitude representation for the mantissa can be used. A feature of the linear array is the ability to multiply operands with arbitrary length exponents.

Systolic ring multiplier: The recurrence relations which define a systolic cell show that only state information is transferred between cells. In addition, only a finite number of input characters k contribute to each output. It is therefore possible to replace the linear array of m cells with a systolic ring of q cells and $k - 2q$ state registers, where $q \leq m/2$. The registers may be lumped or distributed. The k characters of the operands are input into the ring and m recurrences are applied by circulating the operands $[m/q]$ times before outputting the result. The next computation is fully pipelined as new operands are entered into the ring during the output phase. Fig. 3 shows a

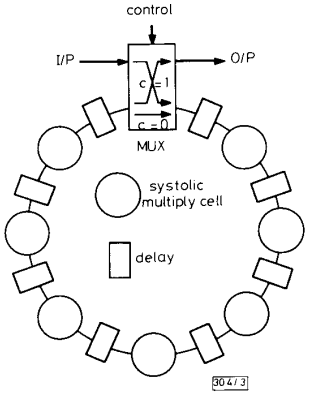

Fig. 3 *Serial systolic ring floating point multiplier*

systolic ring multiplier with distributed state memory. When implemented in this form, the multiplier can process operands of various specifications. For the limiting case where one computational cell is augmented with $k - 2$ delay stages, the multiplier can process floating point operands whose specifications range from $k - 1$ mantissa characters and a single exponent character (i.e., a fixed point multiplier) to $k - 1$ exponent characters and a single mantissa character (i.e., a fixed point adder). This provides a wide range of possible dynamic range and precision options in a single hardware implementation.

Discussion: Systolic ring and linear array floating point multipliers constructed according to the recurrences described in this letter are of interest both in large order systolic arrays and also neural networks. This is because of the wide range of area/time/precision/dynamic-range tradeoffs achievable with the architecture. A one bit per character multiplier for systolic array application has been fabricated in a 2 micron CMOS process and successfully tested at 20 MHz.

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COAX-TO-CHANNELISED COPLANAR WAVEGUIDE IN-PHASE N-WAY, RADIAL POWER DIVIDER

Indexing terms: Waveguides, Transmission lines

A novel nonplanar, wideband power divider which makes use of a coax-to-CCPW transition is demonstrated. The transition utilises a coaxial transformer whose outer conductor is slotted along the length for RF power division and also for exciting the CCPWs in equal amplitude and phase at the radial junction. The measured (8–16 GHz) excess insertion loss at the output ports is 0·5 dB for a four-way divider. The amplitude and phase balance are within 0·5 dB and 5°, respectively. The power divider should find applications in the feed network of phased arrays.

Introduction: Channelised coplanar waveguides (CCPW)[1] are a new variant of the conventional coplanar waveguide (CPW).[2] The CCPW has all the advantages of conventional CPW and also has lower radiation loss. In the conventional CPW, the loss of power by radiation to free space occurs from the printed circuit and the substrate. By embedding the substrate in a channel, the radiation loss from the substrate is suppressed. A practical CPW circuit such as a power divider also has several bend and step type discontinuities which can excite higher order CPW modes and surface wave modes. These modes can propagate if the cross-sectional geometry is favourable and may reduce the isolation between adjacent circuits besides giving rise to insertion loss spikes. The metal channel of the CCPW also acts as an effective barrier against interference through the substrate.

We demonstrate a novel power divider which uses a nonplanar coax-to-CCPW transition. The new design has advantages over the conventional planar, in-line Wilkinson type,[3] power divider. It eliminates the need for right angle bends which require dielectric overlays for phase velocity correction.[4] It eliminates the unreliable and nonreproducible bondwires which are used to tie the two ground planes to the same

potential. It is also capable of simultaneously exciting multiple odd or even number CCPWs in equal amplitude and phase.

Radial junction: A coax-to-CCPW in-phase, four-way radial power divider is shown in Fig. 1. The junction is formed by the intersection of four CCPW lines. Power is coupled to this junction from a coaxial cable whose outer conductor is slotted along the z direction to form four coupled transmission lines. The centre pin of the coaxial line meets the intersecting CCPW centre conductors and the four coupled outer conductors meet the CCPW ground planes. The electric current at the open end of the coax is divided into the four CCPW lines illustrated in Fig. 2. This arrangement has the advantage of holding the ground planes at the same potential and exciting the four CCPW lines in equal amplitude and phase without the need for bond wires. Each of the four CCPW lines, Fig. 3, has an impedance of 135Ω at the junction. The net impedance seen by the coaxial line is approximately 34Ω. A quarter wave coaxial dielectric transformer ($\varepsilon_r = 4$) was used at the junction to match the 50Ω coaxial line to the 34Ω CCPW junction impedance. The characteristic impedance of the quarter wave coaxial dielectric transformer section as determined from Reference 5 is approximately 40Ω. The characteristic impedance ($Z_0 = V^2/P$) of the CCPW line at the output ports was set to 70Ω to provide a good match to the 50Ω coaxial connector.[4] Each of the three pairs of slits in the ground plane of the CCPW (Fig. 3) acts as a tuning stub to improve the CCPW to coaxial connector impedance match over the measured frequency range.

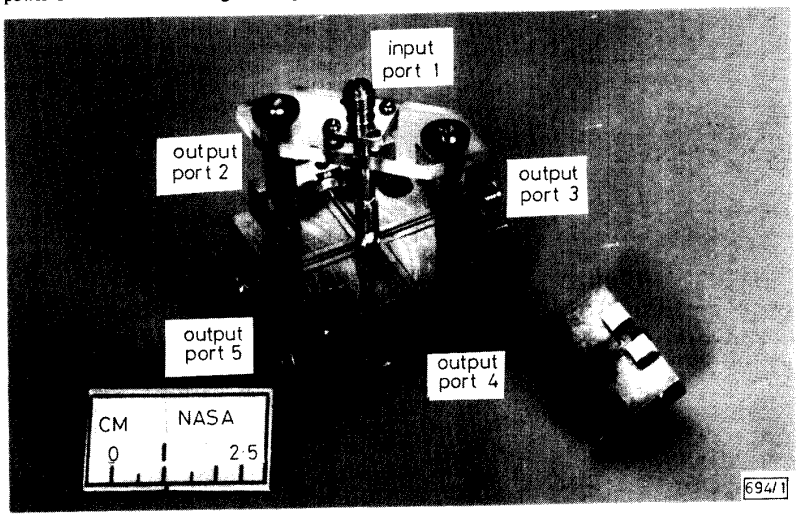

Fig. 1 *Coax to CCPW in-phase, four-way, radial power divider*

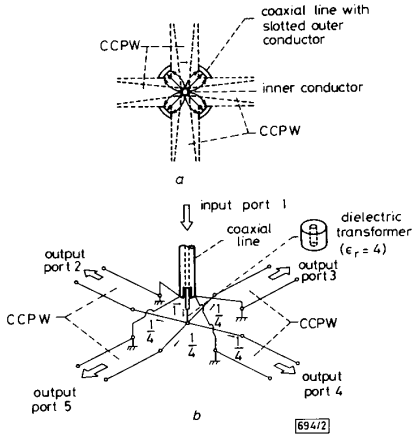

Fig. 2 *Radial power divider characteristics*
a Electric field distribution at end of slotted coaxial line
b Equivalent circuit of junction

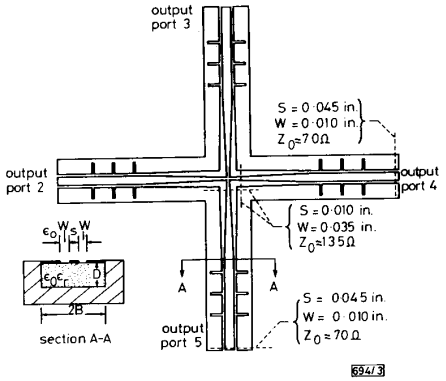

Fig. 3 *Coax to CCPW in-phase, four-way, radial power divider details*

Experimental results: The measured amplitude of the power coupled to one of the output ports over an octave bandwidth (8–16GHz) is shown in Fig. 4 and is typical of the junction. The −6·5dB measured amplitude at the output ports is in good agreement with the −6·0dB expected for a 1 : 4 ideal lossless junction. The additional loss of 0·5dB includes the CCPW to coaxial transformer and two coaxial connector losses. Also superimposed on Fig. 4 is the return loss of the input port which is greater than 10dB. The amplitude and phase balance of this circuit are within 0·5dB and 5°, respectively. These values are a function of the mechanical structure itself since all the ports are identical. The isolation between the ports is approximately 10dB.

Conclusion: The design, implementation and characterisation of a *N*-way, in-phase, radial power divider which employs a novel coax-to-CCPW transition has been demonstrated. This

is the first successful implementation of a copolanar waveguide power divider. The low loss and wide bandwidth characteristics of the divider would facilitate the implementation of

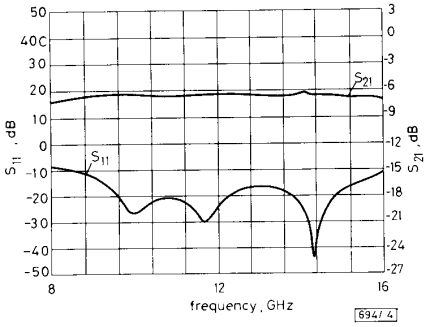

Fig. 4 *Measured coupled power and return loss*

a CCPW feed network in a phased array antenna system. The divider is observed to possess excellent amplitude and phase balance.

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HIGH-SENSITIVITY, HIGH-SPEED InGaAs PHOTOCONDUCTIVE DETECTOR

Indexing terms: Photoelectric devices, Photoconducting devices

$In_{0.53}Ga_{0.47}As$ photoconductive detectors with low dark current and high speed are obtained by multiple energy H bombardment on *p*-type material. The dark current of the detectors is 10 μA, the detectivity at 1·31 μm is 1 A/W and the bandwidth is 1·8 GHz at a source-drain bias of 6 V for 5 μm contact spacing.

$In_{0.53}Ga_{0.47}As$ (InGaAs hereafter) is a useful material for making photodetectors operating in the wavelength range 1·1–1·6 μm. Photoconductors offer some advantages over *pin* photodiodes for photodetection because they can have gains greater than unity and they are simpler to fabricate. But the photoconductive detectors made of *n*-type and *p*-type InGaAs suffer from high dark current and low impulse response speed.[1–3] The dark current problem can be minimised by using Fe-doped high resistive InGaAs.[4] Although the speed of Fe-doped InGaAs detectors is better compared to the *n*- and *p*-type detectors it is still lower compared with the *pin* detectors.

Rao *et al.* have reported an increase in the resistivity of *p*-type InGaAs with H bombardment.[5] For fast response the effective lifetime (τ_{eff}) of the photogenerated carriers in the active device region has to be made as short as possible. A reduction in τ_{eff} might be possible if the lattice damage caused by the H-bombardment introduces recombination centres in the material.[6] Due to these advantages we attempted H-bombardment on *p*-type InGaAs to reduce the dark current to few μA and improve the speed of the photoconductive detector.

A 1·4 μm thick *p*-type InGaAs layer grown by MBE on (100) InP : Fe substrate was used in this study. The net carrier concentration ($N_A - N_D$) in this layer is $5 \times 10^{16}\,cm^{-3}$. Simple source–drain (S–D) Au–Zn/Au ohmic contacts with 5 μm separation and 55 μm width were formed by standard lift-off lithography and alloying. After alloying the ohmic contacts lateral device isolation was achieved by mesa etching down to the InP : Fe substrate using $H_3PO_4 : H_2O_2 : H_2O :: 1 : 8 : 50$ solution. Multiple energy $140\,keV/3{\cdot}9 \times 10^{11}\,cm^{-2}$ H^+, $85\,keV/3{\cdot}5 \times 10^{11}\,cm^{-2}$ H^+, $80\,keV/2{\cdot}7 \times 10^{11}\,cm^{-2}$ H_2^+, $30\,keV/1{\cdot}4 \times 10^{11}\,cm^{-2}$ H_2^+, and $15\,keV/9{\cdot}2 \times 10^{11}\,cm^{-2}$ H_3^+ bombardment was performed on the detector to obtain a uniform lattice damage over the entire depth of the active device region. This multiple implant gives a uniform H concentration of $8{\cdot}5 \times 10^{15}\,cm^{-3}$ over the entire depth of the InGaAs layer.

The dark I–V characteristic of the device is shown in Fig. 1. The dark current at 6 V bias is 10 μA. This current is

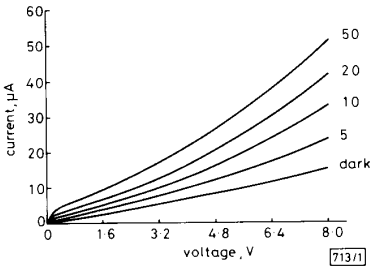

Fig. 1 *I–V characteristics of H-bombarded p-type InGaAs photoconductor*

extremely small when compared with a dark current of 4·32 mA before H bombardment at the same bias voltage. This dark current of 10 μA at 6 V bias is the lowest value reported to date in InGaAs photoconductive detectors of comparable geometry. The decrease in the dark current is caused by the donor levels introduced by the H-bombardment compensating the acceptors in *p*-InGaAs. Though the dark current showed a tendency to saturate at low voltages it kept increasing at high voltages. The dark current is expected to saturate at high fields because of carrier velocity saturation before breakdown. But, probably because of space-charge injection from the contacts, the current increased with an increase in the bias voltage.[7] Heating of the device at high voltages may also contribute to the increase in current. Since dark current in the H-bombardment detectors is low, the thermal noise in these detectors is expected to be much lower when compared with the detectors without H-bombardment. The decrease in thermal noise is expected to improve the sensitivity of the detector.

The DC I–V characteristics of the detector at various laser light (1·31 μm) intensities are also shown in Fig. 1. At 6 V bias, $I_{ph}(I_{total} - I_{dark})$ is 5 μA for 5 μW laser power. This corresponds to a photodetectivity of 1 A/W. I_{ph} increased almost linearly with laser power at all bias voltages for 10 μW laser power in comparison with 5 μW laser power. I_{ph} did not vary linearly with laser power at higher laser powers. In this respect photoconductive detectors are different from metal–semiconductor–metal (MSM) photodetectors.[8]

The impulse response of the photodetector was tested at 1·31 μm using 45 ps width laser at a repetition rate of